Information
• Classroom: 미정
• Class hours: 미정
• Instructor:
  – 박세웅, 880-8414 (132 동 201 호), sbahk@snu.ac.kr
  – Office hours: 미정
• TA: (수업) 이관석 (gslee@netlab.snu.ac.kr)
• Grading:
  – 추후공지
• Prerequisites: none
• Text:
  – 전기공학부 실험 교재 "논리설계 및 실험"
• Homepage:
  – http://netlab.snu.ac.kr/
  – 실험 페이지는 별도

Course Outline
• About the course
  – It covers basic theories of logic circuits including Boolean algebra and logic minimization and operation principles of logic devices. It also covers design methods for combinational logic and sequential logic.
• Schedule (Tentative)
  – 9/1 Introduction I (Ch.1)
  – 3 Introduction II (Ch.1)
  – 8 Boolean algebra I (Ch.2)
  – 10 Logic gates (Ch.2) 9/15 (휴강)
  – 17 Boolean expression (Ch.2)
  – 22 Karnaugh map method (Ch.2)
  – 24 Multi-level logic - AND-OR-Invert/OR-AND-Invert (Ch.3)
  – 29 Gate delay, hardware description languages (Ch.3)
  – 10/1 Steering logic - multiplexers, demultiplexers (Ch.4), Programmable Logic Device - PLA, PAL, ROM (Ch.4)
  – 6 Combinational logic design – examples (Ch.5)
  – 8 Combinational logic design – examples (Ch.5),
  – 13 Arithmetic circuits – Adders (Ch.5)
15 Arithmetic circuits – ALUs, multipliers (Ch.5)
15 Combinational logic design – Number system - binary numbers, hexadecimal/octal numbers, binary arithmetic, ones' complement, two's complement, excess code, BCD, Gray code, ASCII (App.A)
20 Midterm
22 Sequential logic – latches (Ch.6)
22 Sequential logic – flip-flops (Ch.6)
27 Sequential logic - timing (Ch.6)
29 Sequential logic - registers, counters (Ch.6)
11/3 Finite State Machine - concept, design procedure (Ch.7)
5 Finite State Machine - Moore and Mealy machine (Ch.7)
10 FSM optimization - state minimization (Ch.8)
17 FSM optimization - state assignment (Ch.8)
19 Sequential logic implementation (Ch.9)
24 Sequential logic examples (Ch.10)
26 Sequential logic examples (Ch.10)
26 Memories - ROM, SRAM, DRAM (Ch.10)
12/1, 3 (휴강)
12/8 Final exam

- 실험 스케줄은 별도 공지